



Description

JTAC20xM is a thyristor driver with zero-crossing detection function built-in. Several protection features are embedded to ensure reliable and safe system operations: over-temperature shut-down, over-voltage clamping. The device is powered from VDD pin. As soon as the change in the polarity of the V_{AC} line voltage (i.e. zero point) appeared at ZCD pin is detected, the external thyristor can be triggered almost instantly. Eliminating the dead angle of thyristor in the traditional drive circuit and reducing the influence of EMI on the power supply. In practice, the device allows any MCU implemented in low-voltage CMOS process to operate a thyristor which typically cannot be triggered properly by CMOS-level control signal. After the chip detects the zero-crossing signal (Mode 1 and Mode 3), the GATE will automatically pull up to the VDD value if EN is not enabled, then improving the anti-interference ability of the thyristor.

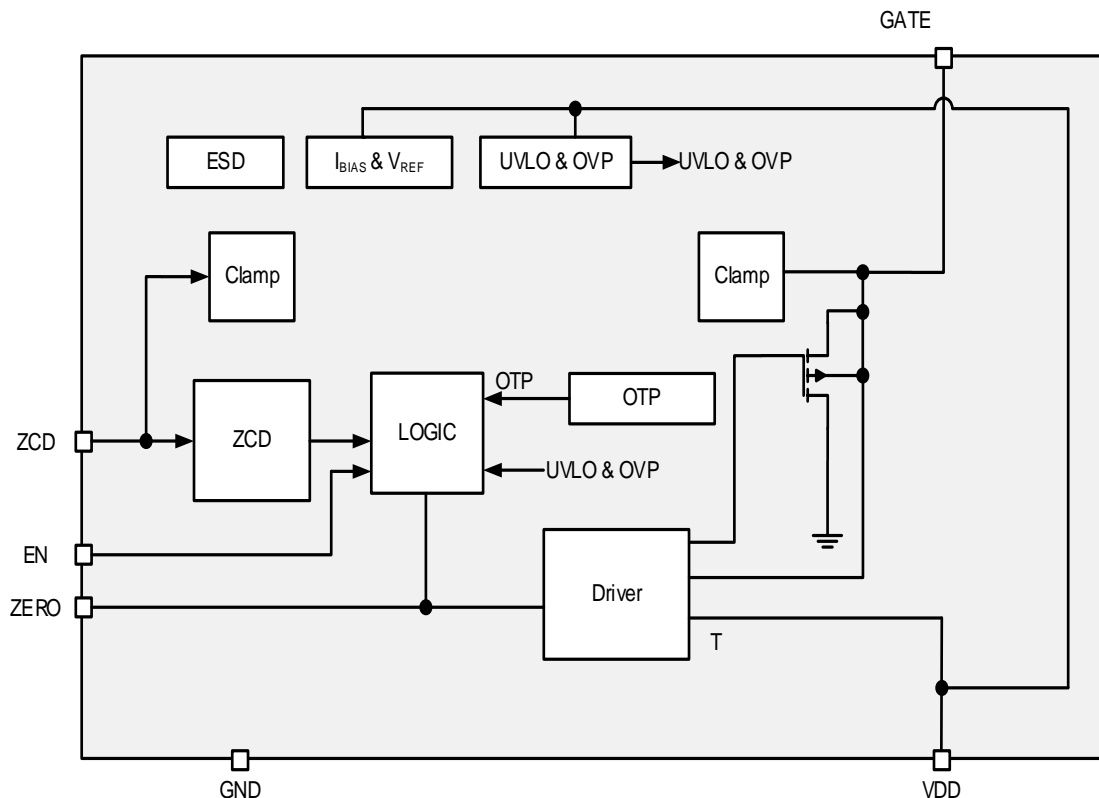
Characteristic

- Zero-crossing detection
- Enhanced ESD performance
- Over-temperature shut-down
- VDD over-voltage clamping
- Negative output

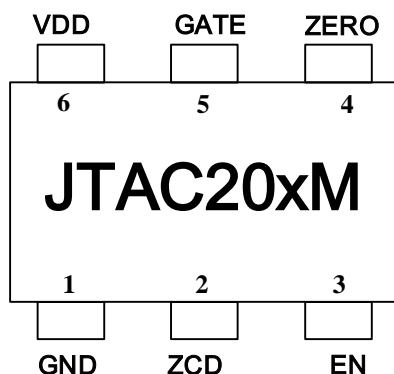
Application Range

- Home appliances
- Electric Power Tool
- Industrial control

Logic Diagram



Pin Distribution and Description



Number	Name	Description
1	GND	Ground terminal
2	ZCD	Zero-crossing detection terminal
3	EN	Enable-control terminal
4	ZERO	Zero-crossing signal output terminal
5	GATE	G pole
7	VDD	Power supply terminal (T1 pole)

Maximum Rating

Parameter	Range
VDD、GATE voltage	$V_{OVP}-1V$
ZCD、EN、ZERO voltage	-0.3 V ~ 5.5V
min./max. junction temperature T_J	-40 °C ~ 150 °C
min./max. ambient temperature T_A	-40 °C ~ 85 °C
min./max. storage temperature T_{stg}	-55 °C ~ 150 °C
soldering temperature (soldering tin, 10secs)	260 °C
VDD voltage range recommended	-0.3V ~ 15V

ELECTRICAL CHARACTERISTICS ($V_{DD}=6V$, $T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Condition	MIN.	TYP.	MAX.	Unit
Supply voltage (VDD voltage)						
$I_{Start-up}$	Start-up current	$V_{DD}=3V$		350		μA
I_{Static}	Static current	$V_{DD}=5.5V$		800		μA
$UVLO_{(ON)}$	Under-voltage lockout _(ON)	VDD voltage drop		3.5		V
$UVLO_{(OFF)}$	Under-voltage lockout _(OFF)	VDD voltage rise		4		V
V_{DD-OP}	Power supply operating voltage range		4.8	5	6.5	V
OVP	Overvoltage protection voltage		16	18	20	V
V_{DD-max}	Clamping voltage		18	20	22	V
Zero-crossing detection (ZCD)						

T_{Delay}	Delay time			35		μs
I_{ZCD}	Detection threshold	$V_{DD}=5V$		2.1		μA
I_{ZCD_HYS}	Detection threshold hysteresis			0.7		μA
V_{Zcd_clamp}	Internal clamping			0.35		V
Thyristor driver (GATE)						
I_{GATE}	Trigger drive current A			15		mA
	Trigger drive current B			30		mA
	Trigger drive current C			60		mA
	Trigger drive current D			90		mA
	Trigger drive current E			150		mA
R_{Off}	Off state impedance between the G and T1 poles			1.5		Ω
G_{Count}	Number of trigger pulse			6		Cycle
G_{Cycle}	Period of trigger pulse			200		μs
G_{Duty}	Duty cycle of trigger pulse			50		%
Over-temperature protection (OTP)						
T_{Up}	Temperature point			150		$^{\circ}C$
T_{Down}	Recovery point			135		$^{\circ}C$
Enable (EN)						
EN_H	EN high power level			2		V
EN_L	EN low power level			0.4		V

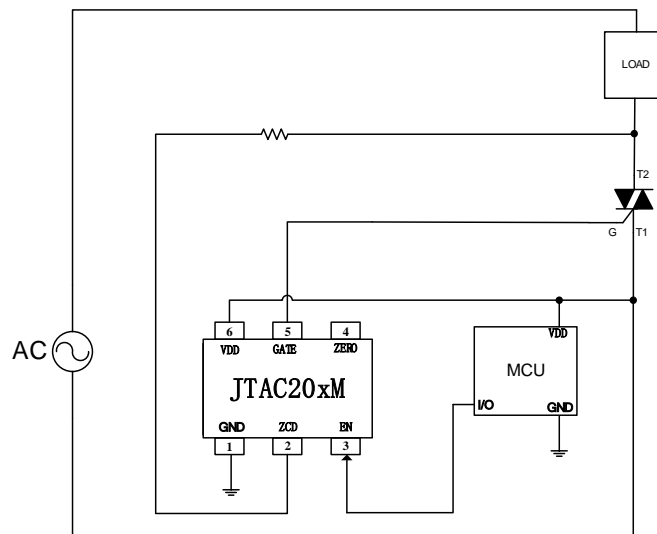
Functional Mode Description

To meet the needs of different customers, JTAC20xM is designed to work under three modes. The connection relationship and functional mode sequence diagram are as follows.

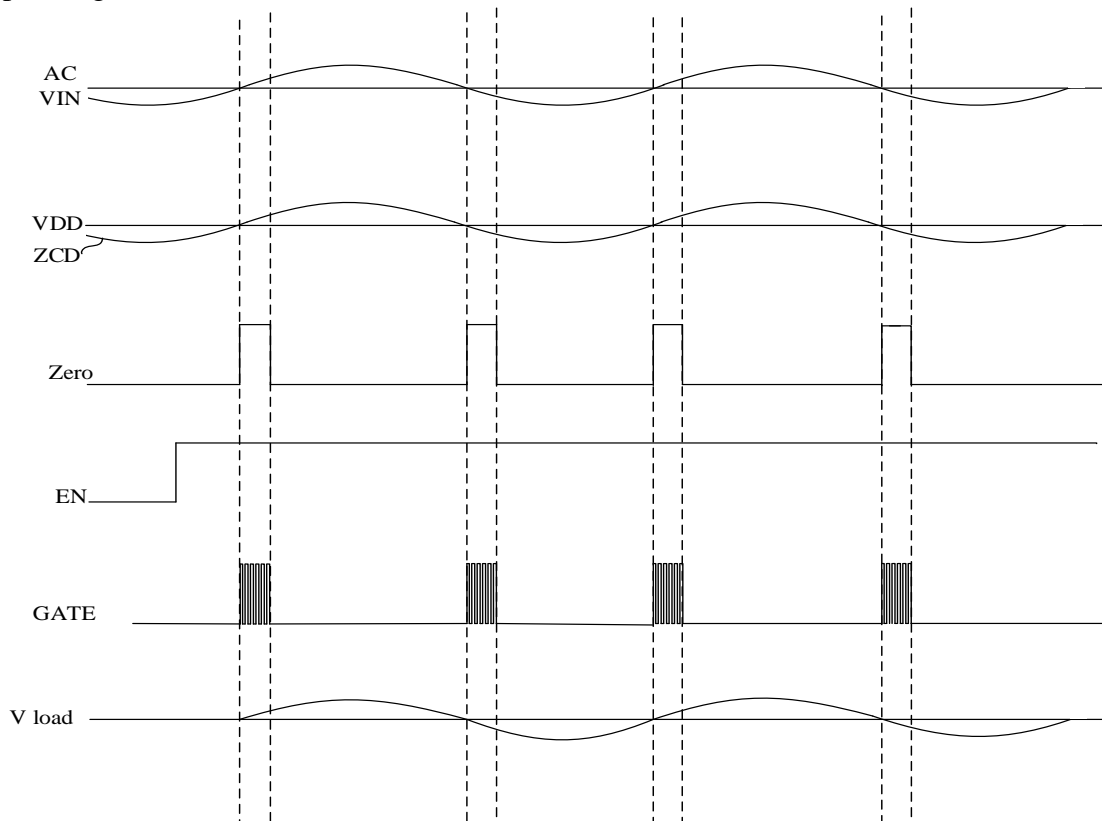
1、 Mode 1

The chip uses common power supply mode, ZCD is connected to AC power line or load terminal through resistance. The pin is used for zero-crossing detection. MCU always outputs high power level to enable chip EN, or EN directly connects to high power level. At each zero-crossing of the chip, ZERO outputs the signal (1.2ms square wave), while the GATE outputs the driving signal (6 cycles of 200us, 50% square wave) to drive the thyristor work.

Schematic circuit diagram:



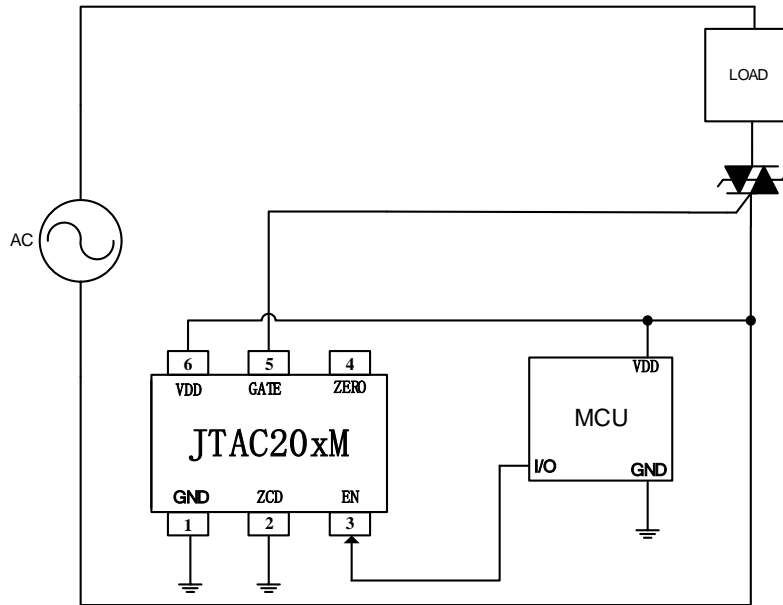
Operating waveform:



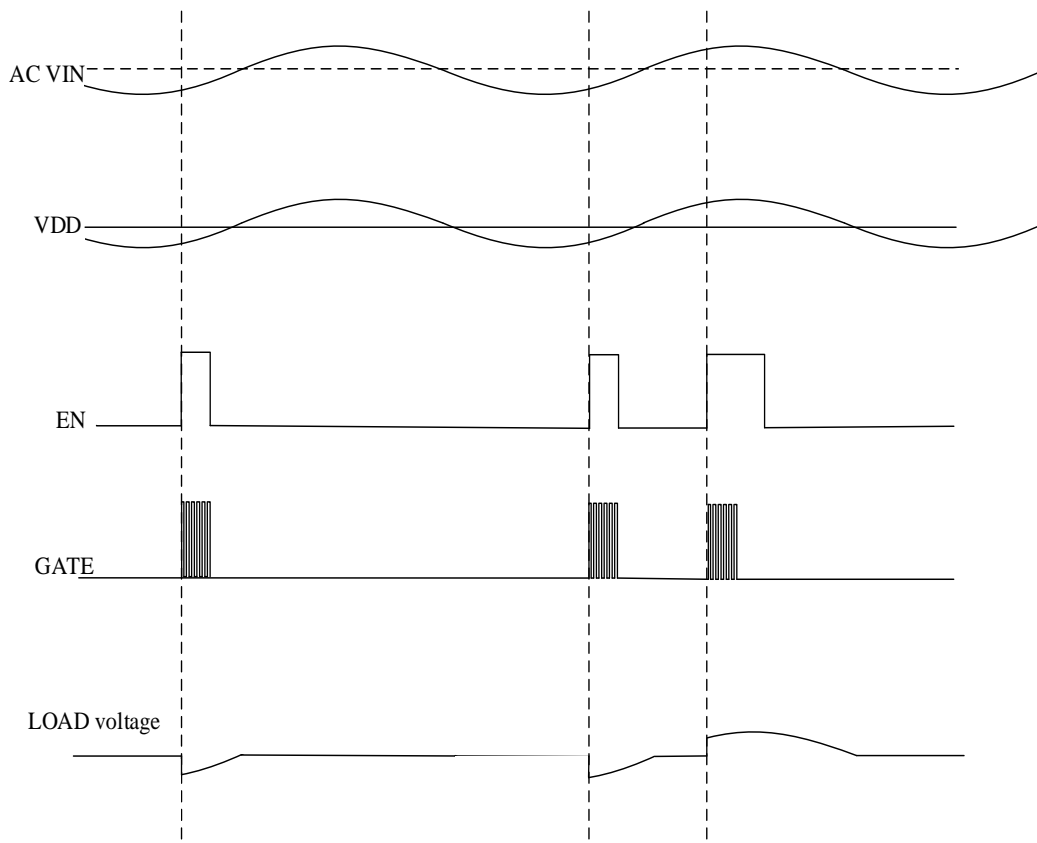
2、 Mode 2

The chip uses common power supply mode, when the ZCD is grounded, the chip shields the zero-crossing detection function, and the GATE driver signal is only controlled by the EN signal. When the EN signal output by the MCU to the chip is high, the GATE will output the drive signal (6 cycles of 200us, square wave with 50% duty cycle) and trigger the thyristor work. In order to ensure the full turn-on of the thyristor, the high level maintenance time of the EN is at least longer than the drive signal time of the GATE. When the MCU output EN signal is low, the GATE will stop the output drive signal, and the thyristor will remain closed when the next AC voltage crosses zero.

Schematic circuit diagram:



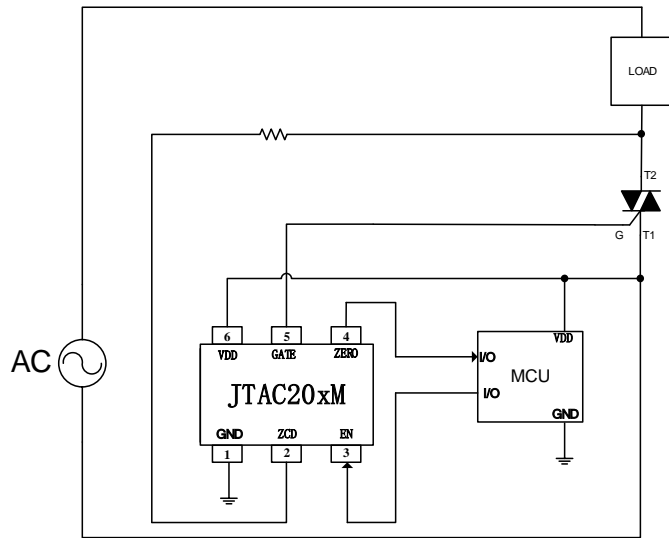
Operating waveform:



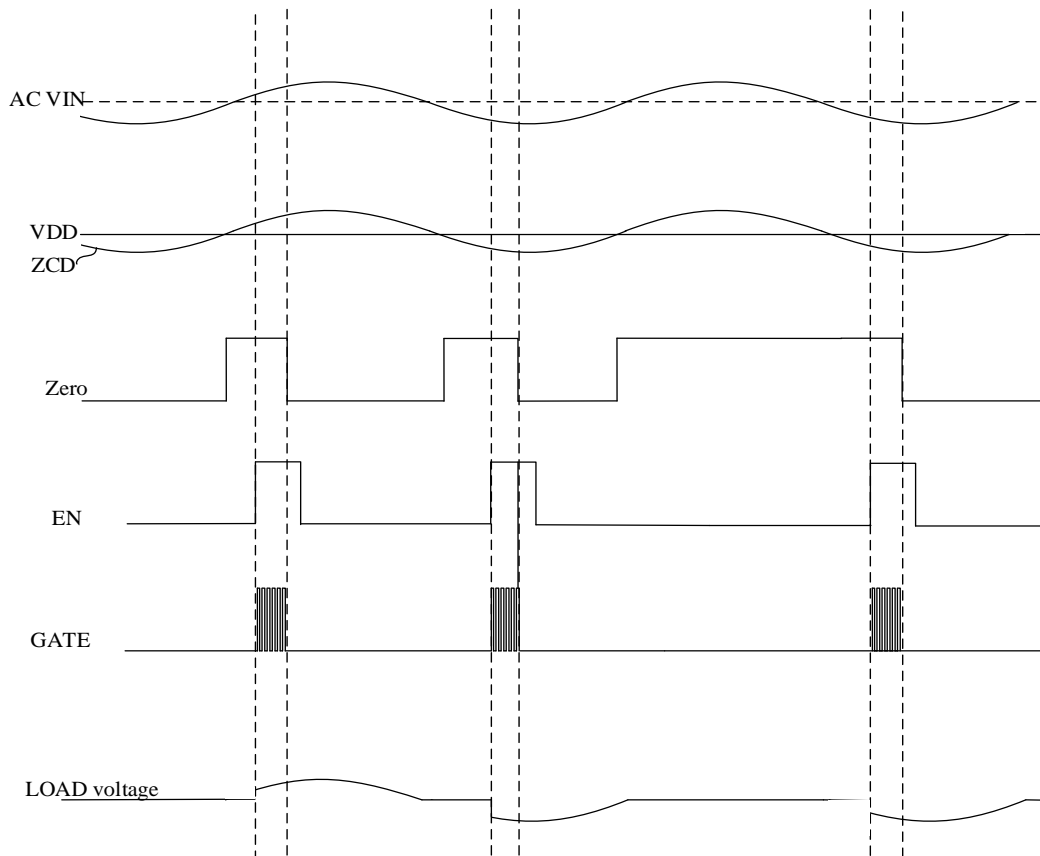
3、 Mode 3

The chip uses common power supply mode, ZCD is connected to AC power line or load terminal through resistance. The pin is used for zero-crossing detection. When the chip detection crosses the ZERO, ZERO outputs the zero-crossing signal to the MCU. According to the zero-crossing signal provided by the chip, the MCU can output the EN high level enable signal immediately or after the corresponding delay, and feed back to the chip. At this time, the GATE end of the chip outputs the drive signal (6 cycles of 200us, square wave with 50% duty cycle) and trigger the thyristor work. In order to ensure the full turn-on of the thyristor, the high level maintenance time of the EN is at least longer than the drive signal time of the GATE. When the MCU output EN signal is low, the GATE will stop the output drive signal, and the thyristor will remain closed when the next AC voltage crosses zero.

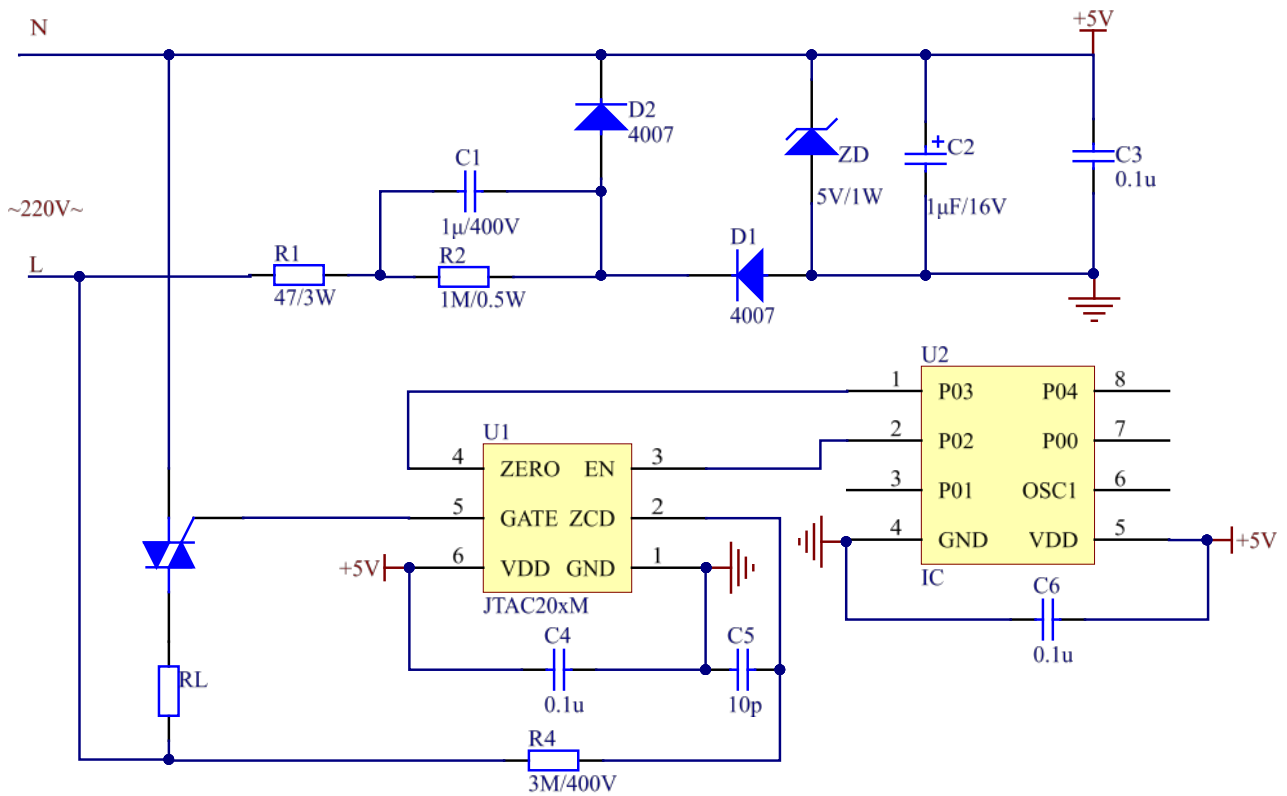
Schematic circuit diagram:



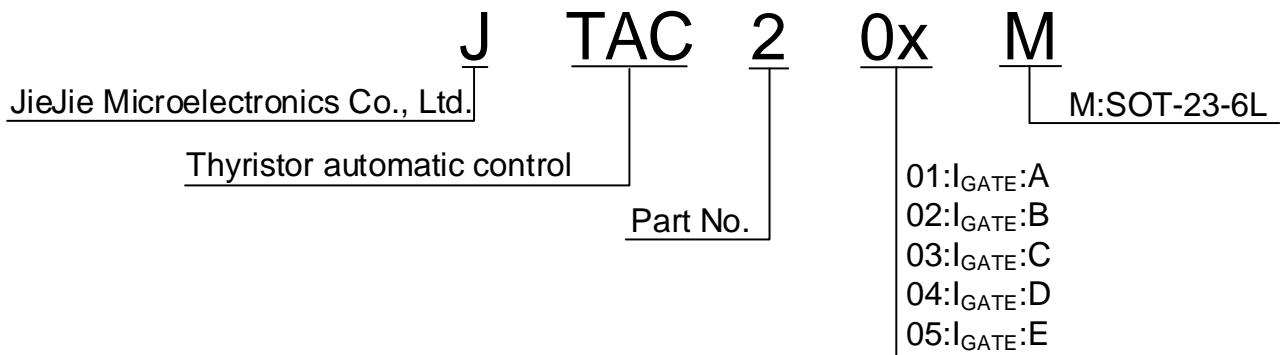
Operating waveform:



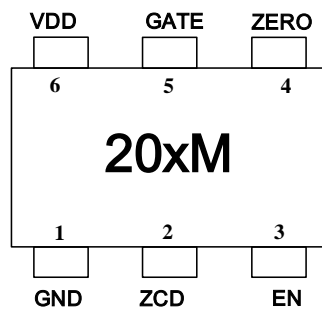
TYPICAL APPLICATION CIRCUIT



NAMING RULE



MARKING



Note: "X" is marked according to the current gear of the GATE actually produced.

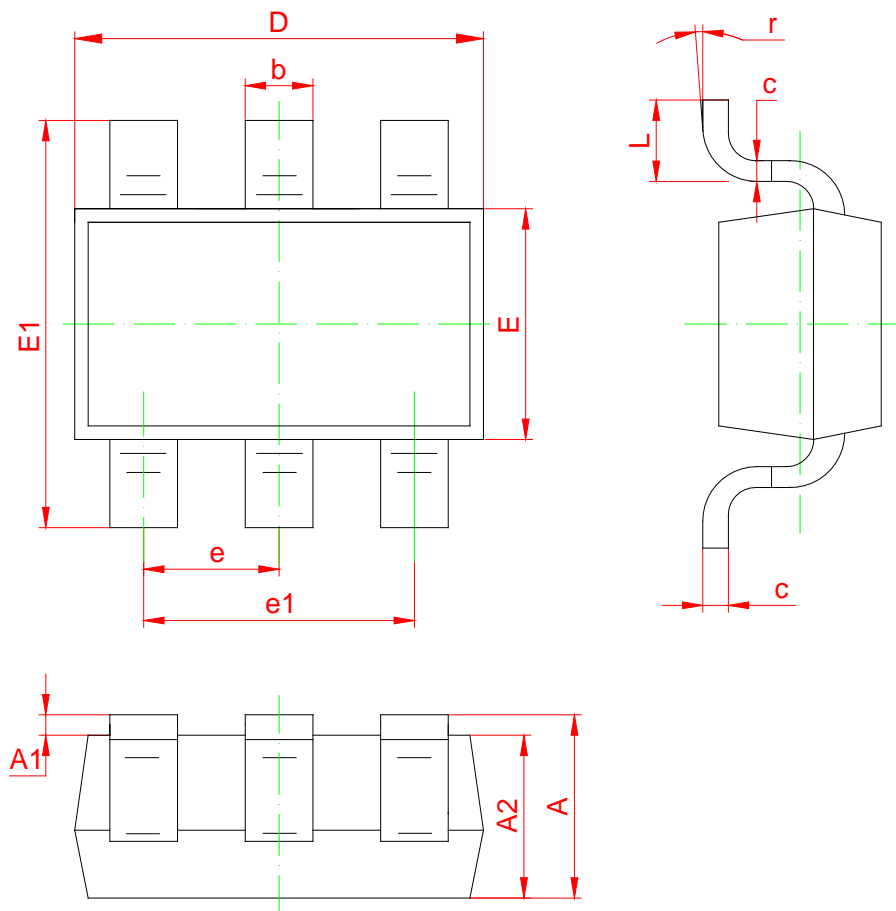
ORDERING INFORMATION

Order code	I _{GATE}	Package	Base qty. (pcs)	Delivery mode	MPQ (pcs)	MOQ (pcs)
JTAC201M	A	SOT23-6L	3,000	Tape and Reel	30,000	120,000
JTAC202M	B	SOT23-6L	3,000	Tape and Reel	30,000	120,000
JTAC203M	C	SOT23-6L	3,000	Tape and Reel	30,000	120,000
JTAC204M	D	SOT23-6L	3,000	Tape and Reel	30,000	120,000
JTAC205M	E	SOT23-6L	3,000	Tape and Reel	30,000	120,000

Document Revision History

Date	Revision	Changes
May.07, 2023	1.0	Last update


PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
r	0°	8°	0°	8°

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co., Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied.

 is a registered trademark of Jiangsu JieJie Microelectronics Co., Ltd.

Copyright © 2023 Jiangsu JieJie Microelectronics Co., Ltd. All rights reserved.